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Improving Power Line Utilization and Performance With Facts Devices In Disturbed Power Systems

M. Siva Sankar[1]

[1] Assistant Professor,Department of EEE, Santhiram Engineering College, Nandyal, Andhra Pradesh, India,

siva.sankar204@gmail.com

Abstract

This Paper describes the theory and simulation by mat lab of flexible Alternative Current Transmission Systems (FACTS) devices used in the disturbed power systems. One of these devices, Unified Power Flow Controller (UPFC) will be chosen for a specific application, detailed in this Project. Simulation investigate the effect of UPFC on the voltage of the related bus, it also considers the effect on the amount of active and reactive power flowing through the transmission system.

Finally simulation results have been presented to indicate the improvement in the performance of the UPFC to control voltage in disturbed power systems.

Key word : FACTS, Disturbed power systems, UPFC, Interfacing, Modeling

1.INTRODUCTION

The term ”FACTS” (Flexible AC Transmission Systems) covers several power electronics based systems used for AC power transmission and distribution. The opportunities arise through the ability of FACTS controllers to control the interrelated parameters that govern the operation of transmission systems including series impedance, shunt impedance, current, phase angle, and damping of oscillations at various frequencies below the rated frequency. Among the FACTS components, Unified Power Flow Controller (UPFC), is the most complete. It is able to control independently the throughput active and reactive powers. The UPFC is capable to act over three basic electrical system parameters: line voltage, line impedance, and phase angle, which determine the transmitted power. In this project, the power flow is controlled by controlling the sending and receiving bus voltage. Also, the control of the shunt and series element of the UPFC will be studied. The Unified Power Flow Controller (UPFC) consists of two voltage sourced converters using power switches, which operate from a common from DC circuit of a DC-storage capacitor.

2. TYPES OF FACTS DEVICES

For the FACTS side the taxonomy in terms of 'dynamic' and 'static' needs some explanation. The term 'dynamic' is used to express the fast controllability of FACTS-devices provided by the power electronics. This is one of the main differentiation factors from the conventional devices. The term 'static' means that the devices have no moving parts like mechanical switches to perform the dynamic controllability. Therefore most of the FACTS-devices can equally be static and dynamic. A power electronic based system & other static equipment that provide control of one or more AC transmission parameters.

3. UNIFIED POWER FLOW (UPFC) CONCEPT

The UPFC is a combination of a static compensator and static series compensation. It acts as a shunt compensating and a phase shifting device simultaneously. The UPFC consists of a shunt and a series transformer, which are connected via two voltage source converters with DC-capacitor.

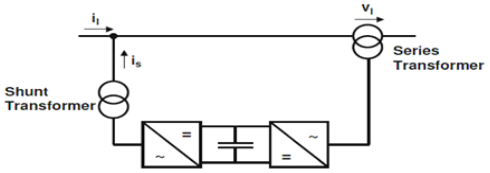


Fig-1: Principle configuration of an UPFC

The DC-circuit allows the active power exchange between shunt and series transformer to control the phase shift of the series voltage. This setup, as shown in Figure, provides the full controllability for voltage and power flow. The series converter needs to be protected with a thyristor bridge. Due to the high efforts for the Voltage Source Converters and the protection, an UPFC is getting quite expensive, which limits the practical applications where the voltage and power flow control is required simultaneously. Terminals of the line or power angle, were controlled separately using either mechanical or other FACTS devices such as a Static Var Compensator (SVC), a Thyristor Controlled Series Capacitor (TCSC), a phase shifter, etc. However, the UPFC allows simultaneous or independent control of these parameters with transfer from one control scheme to another in real time. Also, the UPFC can be used for voltage support, transient stability improvement and damping of low frequency power system

oscillations. Because of its attractive features, modeling and controlling an UPFC have come into intensive investigation in the recent years.

4. UPFC MATHEMATICAL MODEL

In order to simulate a power system that contains a UPFC, the UPFC needs to be modeled. Fig shows a diagram for UPFC; all the variables used in UPFC model are denoted in fig with bold fonts representing phasors. Per unit system and MKS units are jointly used in modeling. The ac system uses par unit system with its variables calculated based on the system-side SB and VB, while the dc variables are expressed in MKS units. We first consider the UPFC dc link capacitor charging dynamics.The current Id1, Id2 and the capacitor voltage and current have the following relation with harmonics neglected

$$\mathbf{I_d} = \mathbf{C}\frac{\mathbf{dV_d}}{\mathbf{dt}} \quad (1)$$

$$\mathbf{I_d} = \mathbf{I_{d1}} + \mathbf{I_{d2}} \quad (2)$$

If we assume the inverters are ideal, the real power exchange with the ac system will be (*P*1 and *P*2 are in p.u.):

$$P_1 = \frac{V_d I_{d1}}{S_B}, P_2 = -\frac{V_d I_{d2}}{S_B} \quad (3)$$

From equation (1) and (2), we have:

$$CC_d = -\frac{dV_d}{dt}(P_1 - P_2)S_B \quad (4)$$

From ac system, we know that *P*1 and *P*2 calculated by:

$$P_1 = R_e(V_1 I_1^*) = R_e\left(V_1\left(\frac{n_1 V_S - V_1}{jX_{11}}\right)^*\right) \quad (5)$$

$$P_2 = R_e(V_{pq} I_1^*) = R_e\left(V_{pq}\left(\frac{V_S + V_{pq} - V_R}{jX_{12}}\right)^*\right)$$

Applying modern PWM control technique two the two voltage source converters, the relations between the inverter dc-and ac-side voltages can be expressed by:

$$V_1 = m_1\frac{V_d}{V_B}, V_2 = m_2\frac{V_d}{V_B} \quad (6)$$

Where coefficient *m1* and *m2* represent the PWM control effects in order to maintain desired inverter ac-side voltages *V1* and *V2* respectively. The desired *m*1 and *m2* are UPFC main control outputs. *V1* and *V2* are in p.u. and *VB* is the ac system base voltage.

The phase angle of (*V1*) and (*V2*) are denoted as (*Θ1*) and (*Θ2*) respectively. They are controlled through firing angle (*φ1*) and (*φ2*) of two converters:

$$\theta_1 = \theta_s - \varphi_1, \theta_2 = \theta_s - \varphi_2 \quad (7)$$

The desired *φ1* and *φ2* are UPFC main control outputs. Finally, taking series transformer ratio into consideration, and rewriting equations (1) to (6), the UPFC power frequency model used in dynamic study will be:

$$CV_d = -\frac{dV_d}{dt}(P_1 - P_2)S_B \quad (8)$$

Where:

$$P_1 = R_e\left(V_1\left(\frac{n_1 V_S - V_1}{jX_{11}}\right)^*\right) \quad (9)$$

$$P_2 = R_e\left(V_{pq}\left(\frac{V_S + V_{pq} - V_R}{jX_{12}}\right)^*\right)$$

$$V_1 = m_1\frac{V_d}{V_B}, V_2 = m_2\frac{V_d}{V_B} \quad (10)$$

$$\theta_1 = \theta_s - \varphi_1, \theta_2 = \theta_s - \varphi_2$$

The desired m1, *φ1, m2 and φ2* can be obtained from UPFC main control system, therefore based on equation (9) together with UPFC control system equations and ac network interface equation.

5. INTREFACE OF UPFC TO THE AC NETWORK

The interface calculation of UPFC to ac network will have significant impacts on transient stability

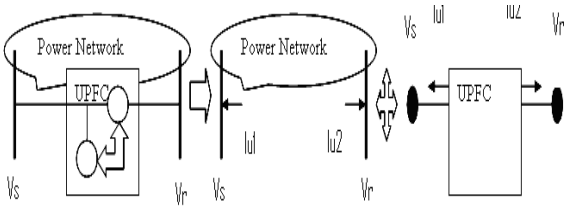


Fig-2: The Interface of the UPFC to the network

In the interface calculation we assume that the bus admittance matrix has been reduced to generator internal buses with UPFC ac terminal buses remained. The corresponding reduced bus admittance matrix takes the form

$$\begin{bmatrix} Y_{GG} & Y_{GU} \\ Y_{UG} & Y_{UU} \end{bmatrix}\begin{bmatrix} E_G \\ V_U \end{bmatrix} = \begin{bmatrix} I_G \\ I_U \end{bmatrix} \quad (11)$$

Where:
EG : Generator internal voltage.
IG : Generator internal current.
VU : ac terminal bus voltages of the UPFC.
The UPFC currents injecting to the ac network can be Expressed by:

$$I_{U1} = -\frac{n_1 V_s - V_1}{jX_{t1}} n_1 - \frac{V_s + V_{pq} - V_R}{jX_{t2}}$$

$$I_{U2} = \frac{V_s + V_{pq} - V_R}{jX_{t2}} \quad (12)$$

Substituting equation (11) into equation (10), and
Re arranging the second equation of equation (10), we finally have:

$$I_{1G} + I_{2G} + \left(Y_{SS} + Y_{RS} + \frac{n_1^2}{jX_{t1}}\right)V_S + (Y_{SR} + Y_{RR})V_R = \frac{n_1}{jX_{t1}}V_1$$

$$I_{2G} + \left(Y_{RS} - \frac{1}{jX_{t2}}\right)V_S + \left(\frac{1}{jX_{t2}} + Y_{RR}\right)V_R = \frac{1}{jX_{t2}}V_{pq} \quad (13)$$

Where:

$$\begin{bmatrix} Y_{SS} & Y_{SR} \\ Y_{RS} & Y_{RR} \end{bmatrix} = Y_{UU}, \begin{bmatrix} I_{1G} \\ I_{2G} \end{bmatrix} = Y_{UG} E_G$$

If we define a constant matrix:

$$Y_{UU} = \begin{bmatrix} \left(Y_{SS} + Y_{RS} + \frac{n_1^2}{jX_{t1}}\right) & \left(Y_{SR} + Y_{RR}\right) \\ \left(Y_{SR} - \frac{1}{jX_{t2}}\right) & \left(Y_{RR} + \frac{1}{jX_{t2}}\right) \end{bmatrix}$$

$$I_U = \begin{bmatrix} \frac{n_1}{jX_{t1}} V_1 - \left(I_{1G} + I_{2G}\right) \\ \frac{1}{jX_{12}} V_{pq} - I_{2G} \end{bmatrix} \qquad (14)$$

We have:

$$Y_{UU} V_U = I_U \qquad (15)$$

The equations from (13) to (14) are used for iteration of UPFC network interface as follows:

a. STEP 1:

Estimates the initials voltages of sending and receiving buses and calculate current based in equations (13) and (9).

b .STEP 2:

Solve equation (14) for difference of the initials voltages values. If the difference is less than the given tolerance for new value of sending and receiving voltages are considered as the solution of equation (12). Otherwise go to step 3.

c. STEP 3:

Update initial voltages and repeat steps 1 and 2 till convergence is reached.

6. SIMULATED TEST SYSTEM

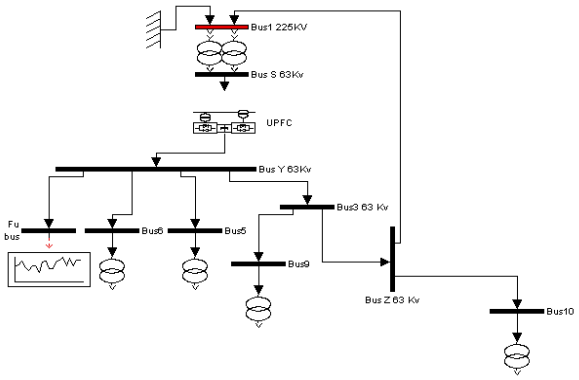
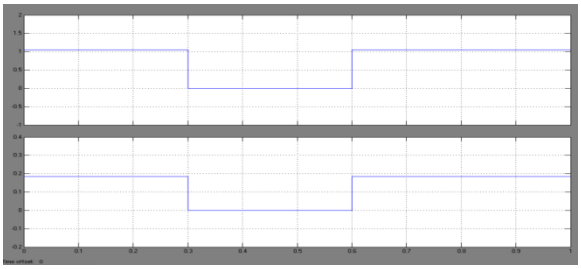


Fig-3: Complex Power System

7. SIMULATION RESULTS

(I) (a). Without UPFC at bus 3



(b). With UPFC at bus3

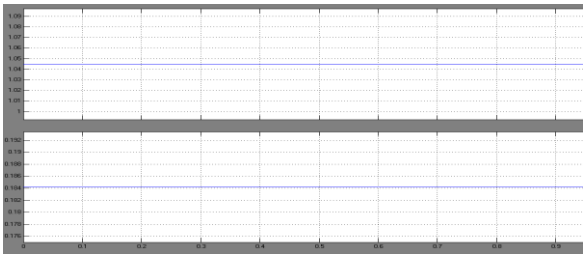
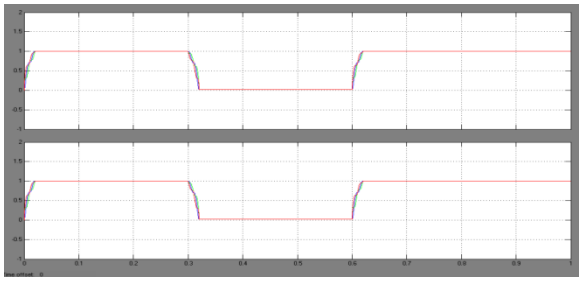


Fig-(I) (A) Active power & Reactive power at bus 3 without upfc
(B) Active power & Reactive power at bus3 with UPFC

(II) (a). Without UPFC at bus 3&4



(b). With UPFC at bus 3&4

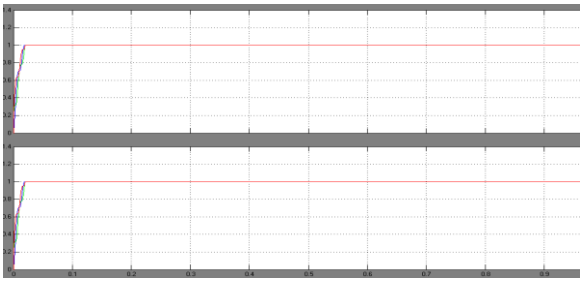
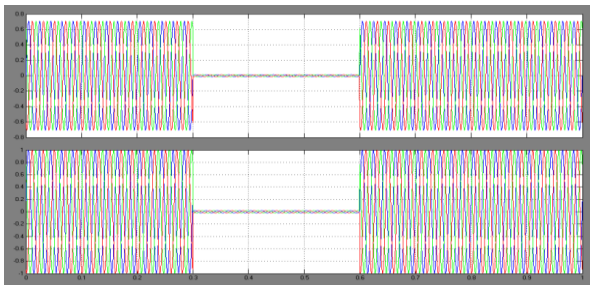


Fig-(II) (A) RMS voltage at bus 3&4 with out UPFC
(B) RMS voltage at bus 3&4 with UPFC

(III) (a). Without UPFC at bus 3&4



(b). With UPFC at bus 3&4

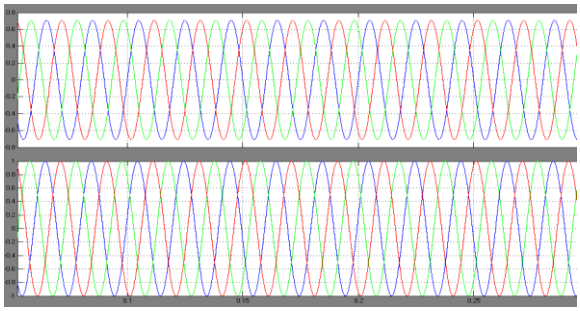
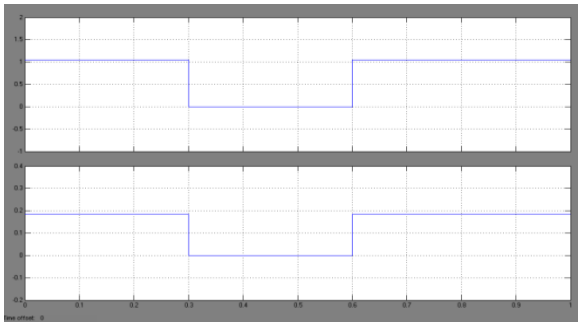


Fig (III) (A) V_{abc} & I_{abc} at bus 3&4 without UPFC
(B) V_{abc} & I_{abc} at bus 3&4 with UPFC

(IV) (a). Without UPFC at bus 4



(b). With UPFC at bus 4

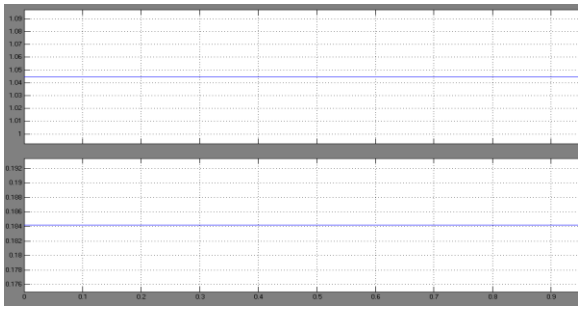
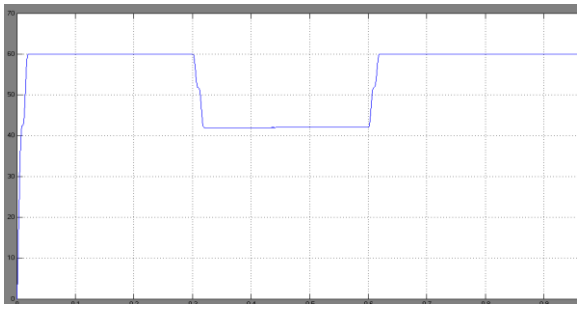
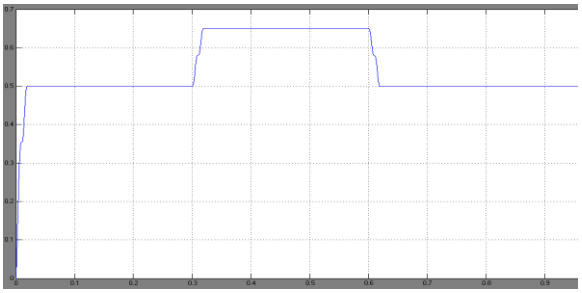


Fig (IV) (A) Active power & Reactive power at bus4 with out UPFC
(B) Active power & Reactive power at bus4 with UPFC

(V) (a). Dc Voltage with UPFC



(b).Series Inserted Voltage With Upfc



8. CONCLUSION

In this project, the simulation results are obtained by Matlab are due to three phase fault in transmission lines with and with out presence of UPFC. The time of fault is from 0.3 to 0.6 as shown results.

The compensation of an electrical system by using UPFC-FACTS device has been studied. Two important coordination problems have been addressed in this project related to UPFC control. One, the problem of real power coordination between the series and the shunt converter control system. Second, the problem of excessive UPFC bus voltage excursions during reactive power transfers requiring reactive power coordination.

The simulation results, obtained by Matlab show the efficiency of UPFC, in controlling line both active and reactive power flow, three phase voltage and current , rms voltage, DC voltage.

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BIOGRAPHIE

1)Matam Siva Sankar, was born in Kurnool, India. He received B.Tech (Electrical and Electronics Engineering) from JNTUniversity, Hyderabad, India, in2009. M.Tech (Power Electronics), from JNTUA, Anantapuramu, India, in 2011. He is working as an Assistant Professor for the college of Santhiram Engineering College, Nandyal, India. His area of intrest is Power electronics applications to Power systems. (siva.sankar204@gmail.com)